# UNIT- II

## TRANSISTOR CHARACTERISTICS (BJT & FET)

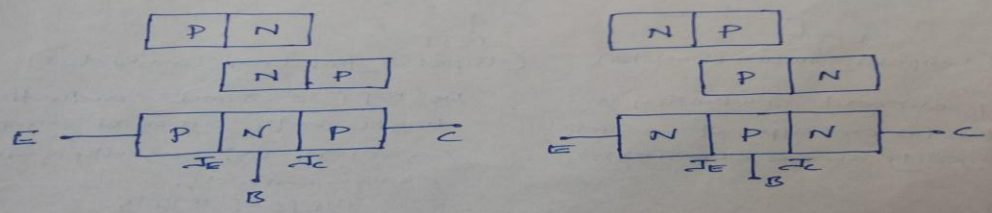
### TRANSISTOR AND FET CHARACTERISTICS

— Before invention of Transistor, Vaccum tube is present which is Bulky, costly and takes more time to conduct. To overcome all these in the year 1947, Transistor was invented by William Shockley. The major advantages of Transistor are:

i) Amplify electronic signals such as Radio & T.V
ii) It has low operating voltage
iii) small size & Ruggedness
iv) Higher efficiency.

### Transistor Construction:

— One PN diode and NP diode are joined back to back which forms a PNP and NPN transistors.




— Transistor is a three terminal device which has Emitter, Base and collector. It has low resistance (maximum current) at input and high resistance (less current) at output of transistor. So transistor came from the word

'TRANSFER RESISTOR' ⟶ TRANSISTOR.

— Transistor:

| | Emitter | Base | collector |
|---|---|---|---|
| Size : | Medium | Small | large |
| Doping : | Heavily | lightly | moderately |

Collector size is large because collector region has to handle more power than the Emitter and therefore more surface area is required for heat dissipation.

— There are two junctions in a transistor $J_E$ & $J_C$.

$J_E$ — It is between Emitter & Base and it is called Emitter-Base Junction or Emitter junction.

$J_C$ — It is between Base & collector and it is called collector-Base Junction or collector Junction.

— there are two types of transistors

- UJT (Unipolar Junction Transistor)
- BJT (Bipolar Junction Transistor)

In UJT current conduction is only due to one type of carriers i.e; majority charge carriers.

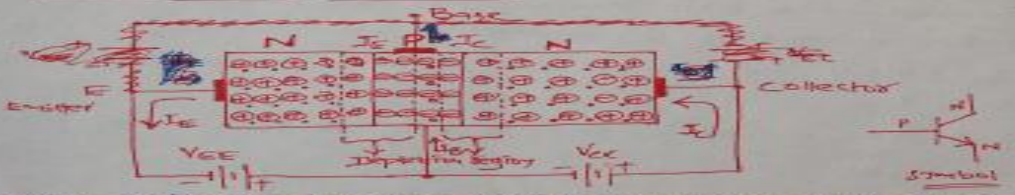
In BJT current conduction is due to both types of charge carriers i.e; majority & minority charge carriers.

Types of BJT's

- NPN
- PNP.

## BJT operation:

### i) operation of NPN Transistor:




— During Diffusion, depletion region penetrates more deeply into the lightly doped side ie; Base inorder to include an equal number of impurity atoms in the each side of the junction.

— For a biased transistor, it is necessary to correctly bias the two P-N junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions.

| Region | Emitter-Base Junction ($J_E$) | Collector-Base junction ($J_C$) |
|---|---|---|
| i) Active | Forward biased | Reverse biased |
| ii) Saturation | Forward biased | Forward biased |
| iii) Cut-off | Reverse biased | Reverse biased |
| iv) Reverse Active | Reverse biased | Forward biased |

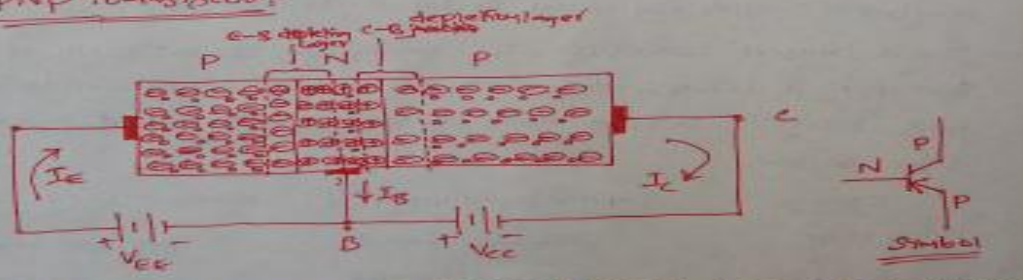
— With D.C source $V_{EE}$ forward biased the depletion region of $J_E$ is reduced and with $V_{cc}$ Reverse biased $J_C$, depletion region of $J_C$ is increased. The forward biased E-B junction causes electrons in N-type to flow towards base constituting emitter current, $I_E$.

As E-B junction is forward bias no current flows through the junction. The Emitter current $I_E$ diffuse through $J_E$ junction and enters into base where some electrons gets recombined in base and before all electrons get recombined the electrons cross the $J_C$ junction and enters into collector because of base small size.

∴ A small current is flown in base and and large current in collector.

∴ For NPN Transistor $\boxed{I_E = I_B + I_C}$

### ii) PNP Transistor:



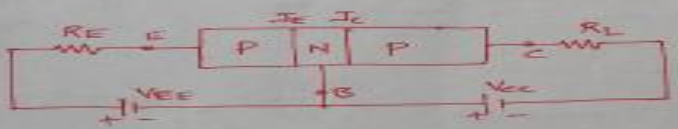

— As Base-Emitter junction is forward biased the majority carriers emitted by P-type emitter flow towards base and constitutes emitter current, $I_E$.

— As Base is N-type there is a chance of recombination of holes emitted by the emitter with the electrons in base. But as base is very thin and lightly doped only few electrons recombine with holes the remaining charge carriers cross over into the collector region to constitute the collector current.

∴ $I_E = I_B + I_C$.

## Transistor as an Amplifier:

The main utility of a transistor is it amplifies the weak signals. The weak signal is applied at input terminals and the amplified output is obtained across the output terminals.




The input circuit is forward biased and has low resistance. A small change in input voltage causes $\Delta V_i$ causes a large change in Emitter current $\Delta I_E$. This causes the same change in collector current and $\Delta I_C$ flows through a high load resistance $R_L$ and a large voltage is developed across $R_L$.

Voltage Amplification $A = \dfrac{\Delta V_{out}}{\Delta V_{in}}$

$= \dfrac{R_L \cdot \Delta I_C}{R_E \cdot \Delta I_E}$

$= \dfrac{R_L \cdot \alpha \cdot \Delta I_E}{R_E \cdot \Delta I_E}$ $\Rightarrow \therefore$ $\boxed{A = \dfrac{\alpha R_L}{R_E}}$

where $\alpha$ is a fraction of current change which is collected.

$\therefore$ $A > 1$ and transistor acts as an amplifier.

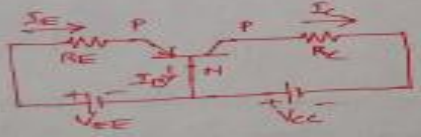
## Transistor Configurations:

The transistor can be connected in a circuit in the following three configurations

- Common Base configuration
- Common Emitter configuration
- Common Collector configuration

### 1) Common Base configuration:

The circuit shows Common Base configuration as Base is common to Emitter and collector terminals.




From the figure: $I_C = \alpha I_E + I_{CBO}$

$\alpha I_E$ — current due to majority carriers

$I_{CBO}$ — current due to minority carriers

since $I_E = I_B + I_C$

$I_C = \alpha (I_B + I_C) + I_{CBO}$

$I_C = \alpha I_B + \alpha I_C + I_{CBO}$

$I_C - \alpha I_C = \alpha I_B + I_{CBO}$

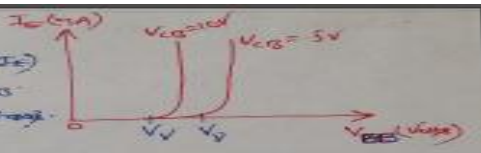
$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$

$$\boxed{I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}}$$

where $\alpha$ is called current amplification factor in CB configuration and $\boxed{\alpha = \dfrac{I_C}{I_E}}$ when no signal is applied.

$\therefore$ $\alpha < 1$. It ranges from 0.95 to 0.995 typical value is 0.98.

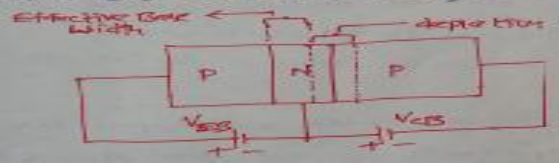
## Input characteristics:




It is the curve between input current($I_E$) and input voltage ($V_{EB}$) at constant $V_{CB}$.
The $I_E$ is taken on Y-axis and $V_{EB}$ on X-axis.
From the characteristics we know:

— After cut-in voltage $V_\gamma$ = 0.2V for Ge & $V_\gamma$ = 0.6V for 'Si', the current $I_E$ increases as $V_{EB}$ increases i.e; input resistance is small.

— With increase in $V_{CB}$ the width of depletion region (B-C) also increases gradually because $V_{CB}$ is reverse biased and the effective Base width decreases which increases $I_E$ current.

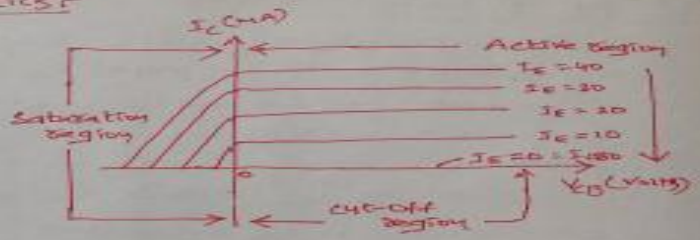



This reduction of effective base width is called "Early Effect" or "Base width modulation".

— This decrease in Base width has two consequences:
i) less chance of recombination in Base region
ii) the charge gradient is increased with in the Base.

— The transistor breakdown occurs when $V_{CB}$ increases beyond certain limit because as $V_{CB}$ increases Effective Base width becomes zero since depletion region spreads completely across base and reaches the Emitter junction $J_E$ where Emitter and collector are shorted. This causes large increase in Emitter current resulting breakdown. This Breakdown is known as "punch-through (or) Reach Through".

## Output characteristics:




— It is the curve between collector current, $I_C$ and collector Base voltage $V_{CB}$ at constant Emitter current, $I_E$.
Output characteristics has three basic regions.
i) Active Region ii) Saturation Region iii) cut-off Region.

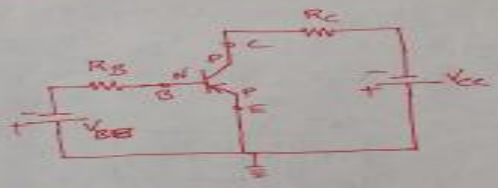
i) Active Region:
In this region $V_{EB}$ is forward biased and $V_{CB}$ is reverse biased and $I_C$ is approximately equal to $I_E$ and transistor works as an amplifier.

ii) Saturation region:
In this region $V_{EB}$ and $V_{CB}$ are forward biased and this curve is represented as left of $V_{CB}$ = 0Volts. There is an exponential increase in collector current $I_C$ as $V_{CB}$ increases towards 0Volts.

iii) cut-off Region:
In this region $V_{EB}$ and $V_{CB}$ are reverse biased. If $I_E$ = 0 then $I_C = I_{CBO}$ a reverse leakage current shown in figure. The region below this $I_E$ = 0 is known as cut-off region where collector current is nearly zero.

## 3) Common Emitter configuration:

— In this configuration Emitter is common to both Base and collector and hence the name Common Emitter configuration.




— We know that

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$$

$$\boxed{I_C = \beta \cdot I_B + (1+\beta) I_{CBO}}$$

As $\beta = \frac{\alpha}{1-\alpha}$ ; $1+\beta = \frac{1}{1-\alpha}$

$\beta \cdot I_B$ is called forward current and $(1+\beta) I_{CBO}$ is called 'Reverse leakage current' in CE configuration and it is denoted as $I_{CEO}$.

i.e; $I_{CEO} = (1+\beta) I_{CBO}$

$I_{CEO} >> I_{CBO}$

& $I_{CEO} << \beta \cdot I_B$.

$\therefore I_C = \beta \cdot I_B + I_{CEO}$ [neglecting $I_{CEO}$]

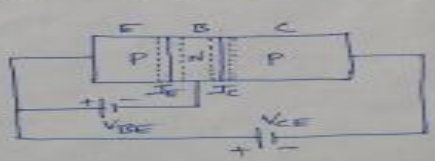
$$\boxed{I_C = \beta \cdot I_B}$$ [neglecting $I_{CEO} = 0$]

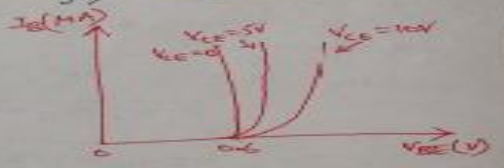
$\therefore$ 'β' is called current amplification factor for CE configuration.

and $\boxed{\beta = \frac{I_C}{I_B}}$ and $\beta > 1$.

### i) Input characteristics:

It is the curve drawn between Input current $I_B$ (Base current) and input voltage $V_{BE}$ (Base-Emitter voltage) keeping output voltage $V_{CE}$ (collector to Emitter voltage) constant.



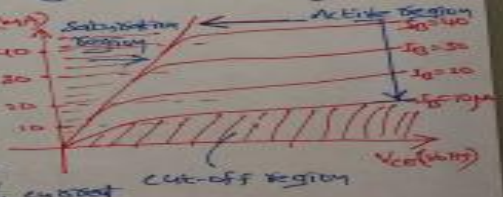

— For $V_{CE} = 0$ V and as $V_{BE}$ is increased the transistor is forward biased and after cut-in voltage $I_B$ increases rapidly.

— For $V_{CE} = 5$V; since $J_C$ is reverse biased the depletion region increases and effective base width reduces and less recombination taking place in base region reducing base current $I_B$ shown in fig. above.

### ii) Output characteristics:

— It is drawn between $V_{CE}$ and $I_C$ keeping input current $I_B$ constant.

— Active region:
In this collector junction $J_C$ is reverse biased. As $V_{CE}$ increases depletion region increases and Base decreases reducing the chance of recombination in the base and $I_C$ current rises more sharply.




— Saturation Region: when both $J_C$ & $J_E$ junctions are forward biased the transistor operates in saturation region shown in fig. above.

— Cut-off Region: when $I_B = 0$; they there is no base and collector current is reverse leakage current $I_{CEO}$ which is shown in figure.

## 3) Common collector configuration:

- In this collector is common to both Base and Emitter and hence it is named common collector configuration.
- We know that

$I_C = \alpha I_E + I_{CBO}$

& $I_E = I_B + I_C$

$I_E = I_B + \alpha I_E + I_{CBO}$

$I_E - \alpha I_E = I_B + I_{CBO}$

$I_E (1-\alpha) = I_B + I_{CBO}$

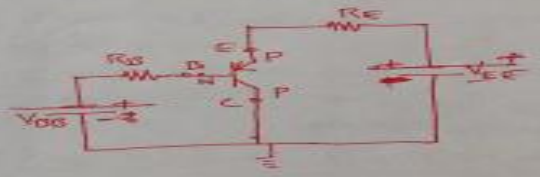
$I_E = \left(\frac{1}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$

$I_E = (1+\beta) I_B + (1+\beta) I_{CBO}$

$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$

$\boxed{I_E = \gamma I_B}$

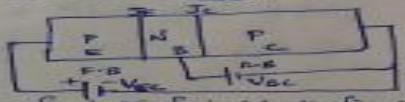
$\boxed{\gamma = \frac{I_E}{I_B}}$




$\frac{\alpha}{1-\alpha} = \beta$; & $\frac{1}{1-\alpha} = 1+\beta$

neglecting leakage current $I_{CBO}$ then

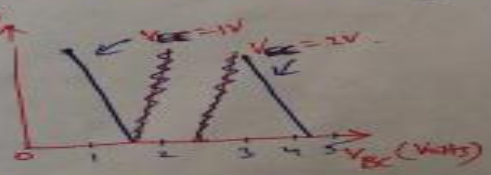
where $\gamma = 1+\beta$.




where '$\gamma$' is called current amplification factor for CC configuration.

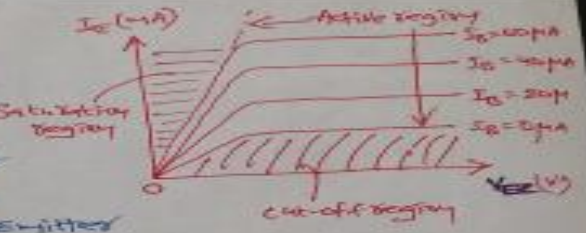
## i) Input characteristics:

- It is the graph between input current $I_B$ Versus input voltage $V_{BC}$ at constant $V_{EEC}$.
- These characteristics are quite different than CB & CE due to input voltage $V_{BC}$ which is largely determined by the level of collector to Emitter '$V_{EE}$' voltage.




## output characteristics:

- The Emitter current $I_E$ is taken along Y-axis and '$V_{EE}$' along X-axis. Since $I_C$ is approximately equal to $I_E$, the common collector output characteristics are practically similar to those of the common Emitter characteristics.




## Comparision of CE, CB and CC configurations:

| | CE | CB | CC |
|---|---|---|---|
| i) Voltage gain, $A_V$ | High | High | Low |
| ii) Current gain, $A_I$ | High | Low | High |
| iii) Input Resistance, $R_i$ | Medium | Low | High |
| iv) Output Resistance, $R_o$ | Medium | High | Low |
| v) Amplification factor | $\beta = \frac{I_C}{I_B}$ | $\alpha = \frac{I_C}{I_E}$ | $\gamma = \frac{I_E}{I_B}$ |
| vi) Application | Audio signal Amplification | Input stage of multi-stage Amplifier | Impedance matching. |

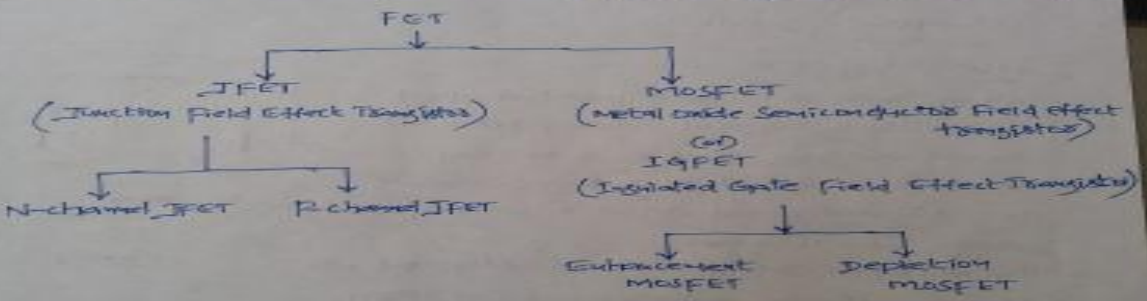
## Why CE configuration is widely used in Amplifier circuits?

i) CE configuration is the only configuration which provides both Voltage gain as well as current gain greater than unity.

ii) In CE the ratio of '$R_o$' to '$R_i$' is small which makes configuration an ideal for coupling between various transistor stages. Maximum power is transferred from stage 1 to stage 2, when '$R_o$' of stage 1 is equal to '$R_i$' of stage 2.

## Field Effect Transistor :-

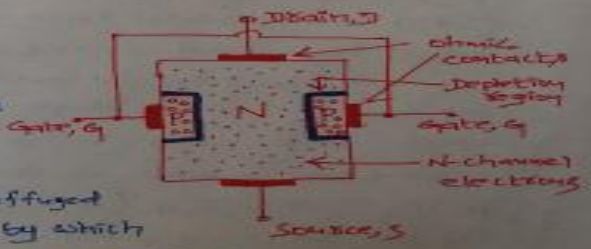
- FET is a semiconductor device which depends for its operation on the control of current by an Electric field.
- FET is a unipolar device, in which current flows only due to majority carriers whereas BJT is a Bipolar device.
- FET is a three terminal device which contains Source (S), Drain (D), Gate (G) and current is controlled by a voltage at gate terminal.




### N-channel JFET :

**construction :**

- It consists of N-type bar which is made of silicon and ohmic contacts are connected with terminals Source and Drain.
- A Heavily doped p-type silicon is diffused on both sides of N-type silicon bar by which pN junctions are formed. These layers are joined together are called Gate, G.




**Source :** Source is a terminal through which majority carriers enter the bar.

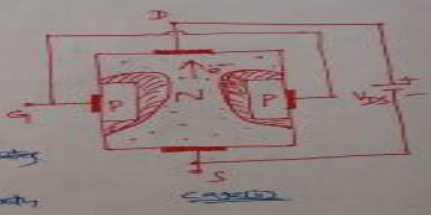
**Drain :** It is the terminal through which majority carriers leave the bar.

**Gate :** Heavily doped 'p' regions of acceptor impurities on both sides of N-type bar have formed.

**channel :** The region between two Gate regions is channel through which majority carriers move from Source to Drain.

**Substrate (or) Shield :** To protect FET from Electromagnetic fields.

**Principle of Operation :**




Case(i) : $V_{GS} = 0$ Volt.

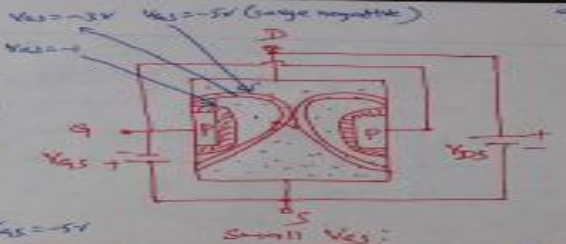
- When there is no Gate potential applied and with $V_{DS}$ applied between Drain and Source electrons start to flow from Source to drain creating daily current, $I_D$. As 'P' is heavily doped depletion region penetrates heavily in to N-channel.
- This depletion region is wider at the top of both p-type material and is narrow at bottom. This is due to Reverse biasing at top side with respect to $V_{DS}$ and forward biasing at bottom side and due to this the shape of depletion region is like wedge shape shown in fig.

Case(ii) : As the voltage $V_{DS}$ is increased from 0 to a few volts, the current will increase as determined by ohm's law. As $V_{DS}$ reaches to $V_P$ (pinch-off voltage) the current is almost constant and this region is called "pinch-off region". The region from 0 to $V_P$ in the graph is called "ohmic Region" and in this region JFET acts like "Voltage Variable Resistor (VVR)".

Case(ii): $V_{GS} < 0$ Volts

— when a negative $V_{GS} = -1V$ is applied the depletion increases and current decreases from what it is at $V_{GS} = 0$ Volt and comes to saturation at lower voltages of $V_{DS}$.

— As $V_{GS}$ is increased more i.e; $V_{GS} = -5V$ both the depletion regions touching at interior zero current flow in the device.




Small $V_{GS}$:

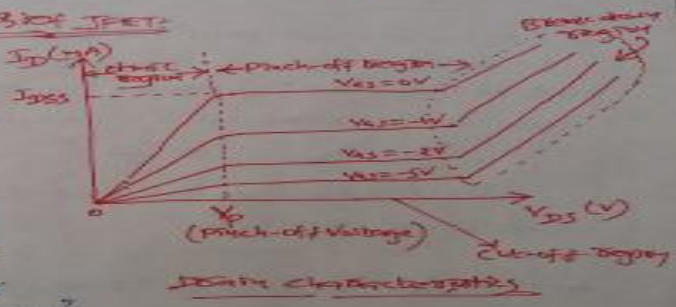
## V-I Amperic characteristics of JFET:

There are two characteristics of JFET they are:

i) Drain (output) characteristics

ii) Transfer characteristics

Drain (output) characteristics:




Drain characteristics

— From the figure as voltage $V_{DS}$ increases there current $I_D$ also increases for small values of $V_{DS}$. This region is called "ohmic region" and FET acts as a "Voltage Variable Resistor (VVR)".

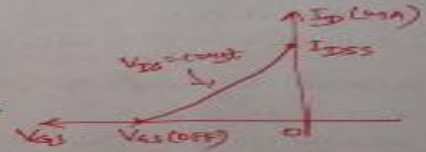
— As $V_{DS}$ increases the current $I_D$ reaches to its constant level called "Pinch-off Voltage, $V_p$" (ii) Constant current region. As $V_{DS}$ is increased beyond "pinch-off" voltage, $V_p$ the drain current $I_D$ remains constant upto certain values of $V_{DS}$ and here space charge region could not oppose the carriers and Reverse current increases and this region is called "Breakdown Region". At this point $I_D$ increases rapidly and the device may be destroyed.

— For N-channel JFET more negative $V_{GS}$ cause $I_D = 0$ where depletion regions completely touches with each other and the channel closes. The value of $V_{GS}$ at the cut-off point is designated as $V_{GS(OFF)}$.

Pinch-off voltage, $V_p$ → constant $I_D$

cut-off voltage, $V_{GS(OFF)}$ → $I_D = 0$.

ii) Transfer characteristics:




— The curve represents transfer characteristics of N-channel JFET relation between $I_D$ and $V_{GS}$ keeping $V_{DS}$ constant.

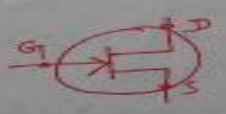
— From the characteristics we have

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

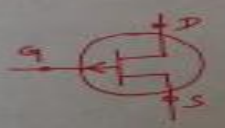
which is non linear and the relationship is defined by "Shockley's" equation.

point at bottom where $I_D = 0$ is $V_{GS(OFF)}$ and at top of curve on $I_D$ axis represents $I_{DSS}$ (Drain-source saturation current) at $V_{GS} = 0$.

Symbols:




N-channel JFET




P-channel JFET

## Parameters of JFET:-

i) Trans conductance ($g_m$):-

$g_m$ = Variation in drain current / Variation in Gate Source Voltage

$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$ | $V_{DS}$ = constant

Units are "micro mhos per Volt" or "MICROSIEMENS"

$\therefore g_m = -\frac{2I_{DSS}}{V_P}\left(1-\frac{V_{GS}}{V_P}\right)$

$\boxed{g_m = g_{mo}\left(1-\frac{V_{GS}}{V_P}\right)}$ $\quad \boxed{g_{mo} = -\frac{2I_{DSS}}{V_P}}$

ii) Drain Resistance, $r_d$:-

$r_d = \frac{\text{drain Voltage}}{\text{drain current}} = \frac{\Delta V_{DS}}{\Delta I_D}$ | $V_{GS}$ = constant

iii) Amplification Factor, $\mu$:-

$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$ | $I_D$ = constant

$= \frac{\Delta V_{DS}}{\Delta I_D} \cdot \frac{\Delta I_D}{\Delta V_{GS}} = r_d \cdot g_m \quad \therefore \boxed{\mu = g_m r_d}$

## Comparison of BJT and FET:-

| BJT | FET |
|---|---|
| 1) current controlled current source | 1) Voltage controlled ~~voltage~~ current source |
| 2) Bipolar device because current flows due to majority & minority. | 2) Unipolar device; current flows due to majority carriers. |
| 3) Input Resistance, $R_i$ is Low | 3) Input Resistance, $R_i$ is High. |
| 4) Bigger in size | 4) Smaller in size used in Integrated circuits. |
| 5) More Noisy | 5) Less noisy than BJT |
| 6) Cheaper | 6) costly |
| 7) "Offset" (or) cut-in Voltage exists | 7) No offset Voltage exists. So it is good for signal chopping. |
| 8) There is Thermal Runaway | 8) No Thermal Runaway |
| 9) $R_o$ increases as output junction is reverse biased | 9) $R_o$ decreases as current passes through the channel. |

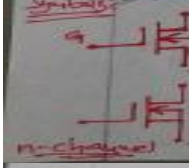
## MOSFET : (Metal oxide Semiconductor FET) (or) IGFET:

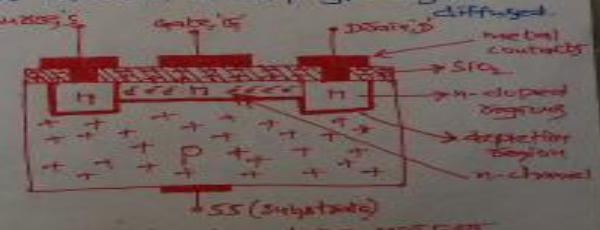
MOSFETs are broken into depletion type and Enhancement type.

### Depletion MOSFET : [N-channel]

**Construction:**

- The basic construction of the n-channel depletion-type MOSFET is provided in figure below.
- A slab of p-type material is formed from a silicon base and is referred to as the "substrate, SS".
- The source and drain terminals are connected through metallic contacts to n-type doped regions linked by an n-channel.
- The gate is also connected to a metal contact surface but remaining insulated from the n-channel by a very thin silicon dioxide ($SiO_2$) layer.
- $SiO_2$ is an insulator referred to as dielectric that sets up opposing electric fields within the dielectric when exposed to externally applied field. The $SiO_2$ provides "no" direct connection between Gate terminal and channel of a MOSFET.
- The reason for label "metal-oxide-semiconductor FET" is:
  metal - for source, drain and gate connections to proper surface
  oxide - for silicon dioxide insulating layer
  semiconductor - for basic structure on which 'n' and 'p-type regions are diffused.
- The insulating layer between the gate and channel has resulted in another name for the device called Insulated-Gate FET (IGFET).

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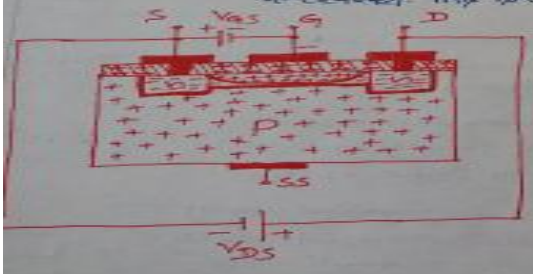
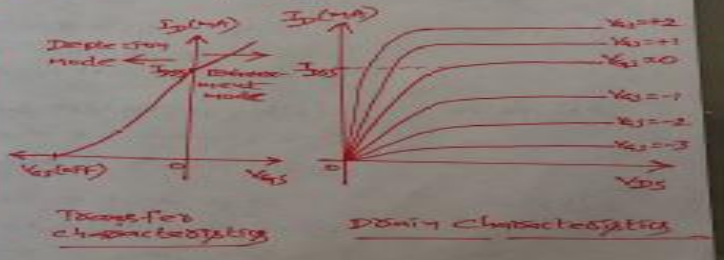
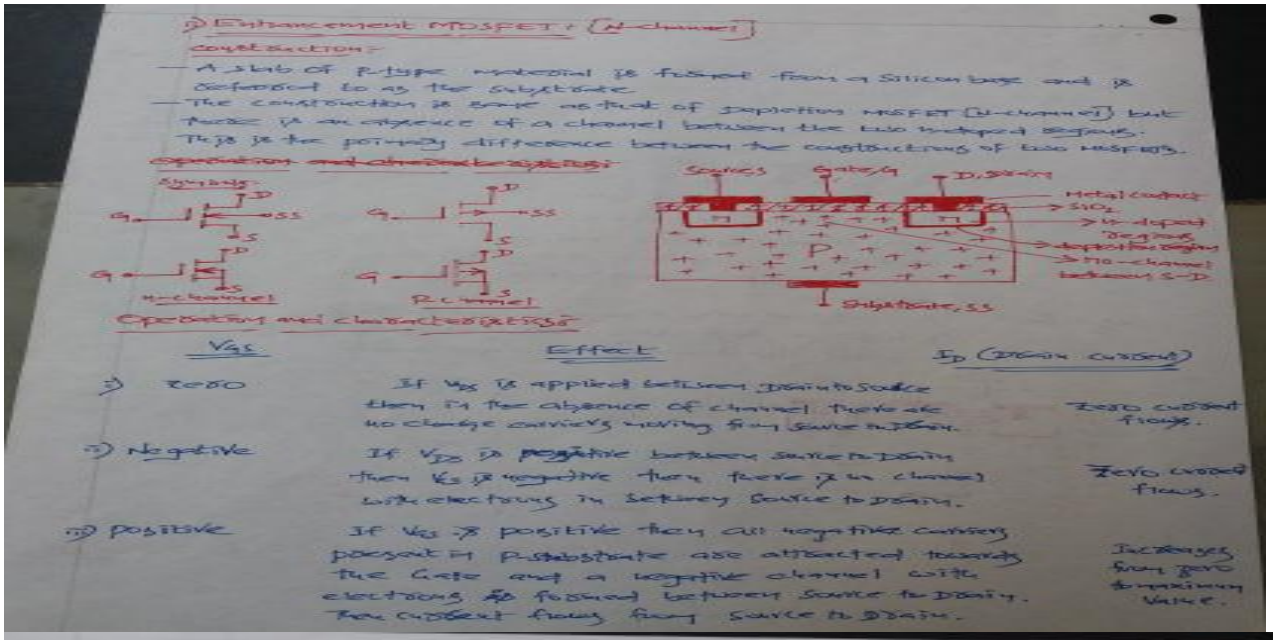
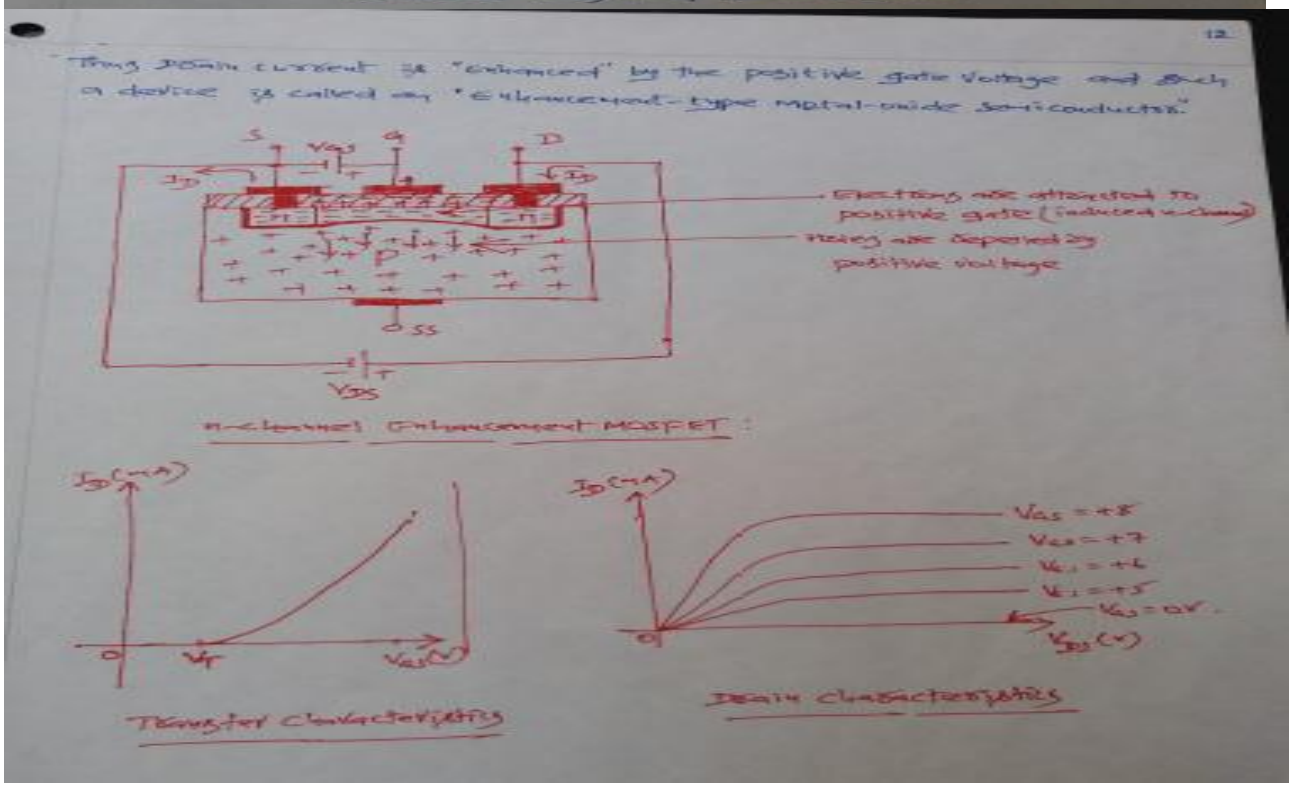
### Operation and characteristics:

| $V_{GS}$ | Effect | $I_D$ [Drain Current] |
|---|---|---|
| i) Zero | If voltage $V_{DS}$ is applied across Drain-Source current slowly increases from source to drain because electrons in n-type leaves at source leaving through the channel and are attracted at Drain. As $V_{DS}$ is increased Drain current also increases shown in figure. | Increases from zero to maximum value, $I_{DSS}$ |
| ii) Negative | The negative potential at gate attracts holes from P-type substrate and repel electrons. Depending on magnitude of $V_{GS}$ (-ve) recombination takes place and reduce electrons in n-channel. | Drain current decreases |
| iii) Positive | The positive gate draws additional electrons from P-type substrate increasing electrons in n-channel. This is called "enhancement region". | still increases |






**Comparison of JFET and MOSFET**

| | JFET | MOSFET |
|---|---|---|
| 1. | The input resistance is High it is in the range of $10^{8}\Omega$ | The input resistance is Very High it is in the range of $10^{10}$ to $10^{15}\Omega$. |
| 2. | Output Drain resistance is higher (1 MΩ) | Output Drain resistance is lower than JFET (50kΩ) |
| 3. | Operated only in the depletion mode | Operated in both depletion and Enhancement mode |
| 4. | Gate leakage current is of the order of $10^{-9}$ A | Gate leakage current is of the order of $10^{-12}$A |
| 5. | The output characteristics are flatter | The output characteristics are not flatter |
| 6. | Used in VLSI circuits. | Widely used in VLSI circuits than JFET |