UNIT - 1

1. Perform the subtraction operation on 22-7 using 2's complement form.

Sol:- Given subtraction of smaller no. from larger no.

$(22)_{10} = (10110)_2$

$(7)_{10} = (00111)_2$

2|22
2|11-0
2|5-1
2|2-1
1-0

2|7
2|3-1
1-1

Step 1:- Find 2's complement of smaller no.

$(00111)_2 = 11000 + 1$

$= (11001)_2$.

step 2:- Add result to larger no.

$$\begin{array}{r} 10110 \\ \oplus\ 11001 \\ \hline 01111 \end{array}$$

step 3:- Neglect carry.

$\therefore 22-7 = (01111)_2 = (15)_{10}$. $\therefore$ ANS:- $(01111)_2 \Rightarrow (15)_{10}$

→ Simplify $(A'B + A' + AB)'$

$= (A'B)' \cdot (A')' \cdot (AB)'$

$= [(A')' + B'] \cdot (A) \cdot (\bar{A} + \bar{B})$.

$= (A + \bar{B})(A)(\bar{A} + \bar{B})$.

$= (A \cdot A + A\bar{B})(\bar{A} + \bar{B})$

$= (A + A\bar{B})(\bar{A} + \bar{B})$. $= A\bar{A} + A\bar{B} + A\bar{A}\bar{B} + A\bar{B}\bar{B}$.

$= 0 + A\bar{B} + 0 + A\bar{B}$. $= A\bar{B}$.

$\therefore \boxed{(A'B + A' + AB)' = A\bar{B}}$

3) If $143_5 = X_6$ then X is ____.

Sol:- let ① $(143)_5 = (?)_{10}$

② $(?)_{10} = (\ )_6$.

$\Rightarrow$ ① $(143)_5 = (?)_{10} \Rightarrow 1\times5^2+4\times5^1+3\times5^0 = 25+20+3$.

$(143)_5 = (48)_{10}$.

The above eq: is in the form of any radix to decimal.

② $(48)_{10} = (\ )_6 =$

6 | 48
6 | 8 - 0
1 - 2

$= (120)_6$

$(143)_5$

$\therefore \boxed{(X)_6 = (120)_6}$

4) If $1010_2 + 10_2 = X_{10}$, then x is.

$$\begin{array}{r} 1010 \\ +\ \ 10 \\ \hline 1100 \end{array}$$

$(1010)_2 + (10)_2 \Rightarrow (1100)_2 = (X)_{10}$.

The above equation is in the form of any radix to decimal.

$1\times2^3+1\times2^2+0\times2^1+0\times2^0 = 8+4 = (12)_{10}$.

$\therefore \boxed{X = 12}$

5) Write the first 9 decimal digits in base 3.

$(0)_{10} = (00)_3$

$(1)_{10} = (01)_3$

$(2)_{10} = (02)_3$

$(3)_{10} = (10)_3$

$(4)_{10} = (11)_3$

$(5)_{10} = (12)_3$

$(6)_{10} = (20)_3$

$(7)_{10} = (21)_3$

$(8)_{10} = (22)_3$

$(9)_{10} = (100)_3$

3 | 2

3 | 3
1 - 0

3 | 4
1 - 1

3 | 5
1 - 2

3 | 6
2 - 0

3 | 7
2 - 1

3 | 8
2 - 2

3 | 9
3 | 3 - 0
1 - 0

6) Convert the following hexadecimal number to octal, decimal.
(i) $(CA72)_{16}$ (ii) $(1AC8)_{16}$.

(i) $(CA72)_{16} \rightarrow (\ ?\ )_{10} \rightarrow (\ ?\ )_8$

① Hexadecimal to decimal to octal:-

i) $(CA72)_{16} \rightarrow (\ ?\ )_{10}$

A=10
B=11
C=12

$C \times 16^3 + A \times 16^2 + 7 \times 16^1 + 2 \times 16^0 \Rightarrow 12 \times 16^3 + 10 \times 16^2 + 7 \times 16^1 + 2 \times 1.$

$= 49152 + 2560 + 112 + 2 = (51826)_{10}.$

$\therefore \boxed{(CA72)_{16} = (51826)_{10}}$

Hexadecimal to octal:-

$(CA72)_{16} \rightarrow (\ \ )_8.$

(1100 1010 0111 0010)

3 bits form a one group from binary to octal

(1100 1010 0111 0010)

1 4 5 1 6 2

$\therefore \boxed{(CA72)_{16} = (145162)_8}$

$\rightarrow (1AC8)_{16} \rightarrow (\ ?\ )_{10}$ & $(1AC8)_{16} \rightarrow (\ ?\ )_8.$

$(1AC8)_{16} = 1 \times 16^3 + A \times 16^2 + C \times 16^1 + 8 \times 16^0$

$= 4096 + 2560 + 192 + 8$

$= (6856)_{10}$

$\therefore \boxed{(1AC8)_{16} = (6856)_{10}}$

$(1AC8)_{16} = (\ ?\ )_8 = (0001\ 1010\ 1100\ 1000)$

three bits form a one group

$= (15310)_8$

$\therefore \boxed{(1AC8)_{16} = (15310)_8}$

7) Given a = 10101001 and b = 1101. Find: (i) a+b (ii) a-b.

128 64 32 16 8 4 2 1

a = 1 0 1 0 1 0 0 1 = 128+32+8+1 = $(169)_{10}$

8 4 2 1

b = 0 0 0 0 1 1 0 1 = $(13)_{10}$.

(i) a+b = 1 0 1 0 1 0 0 1

1 1 0 1

128 64 32 16 8 4 2 1

1 0 1 1 0 1 1 0

$\Rightarrow$ 128+32+16+4+2

$\Rightarrow (182)_{10}$

verification:- 169+13 = (182).

(ii) a-b.

2's compliment of 'b' = 00001101

1's comp = 11110010

2's " = 11110011 $\Rightarrow$ a = $(169)_{10}$.

a-b :- 10101001

a-b = 11110011

10101001

① 10011100

$\therefore$ a+b = 10110110

$\therefore$ a-b = 10011100

(iii) a*b = 10101001 × 1101

10101001

00000000

10101001

10101001

① 10001001 0101

(iv) a ÷ b.

1101) 10101001 (1101

1101

01000 0

1 1 1 0 1

0 0 0 1 1 0 1

1 1 0 1

0

$\therefore$ a+b = 10110110

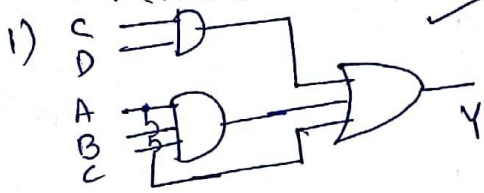
a*b = 10001001 0101

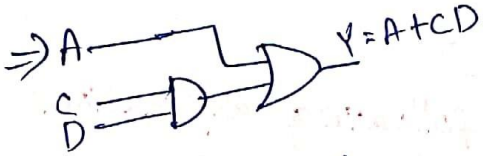
a-b = 10011100

a÷b = 1101

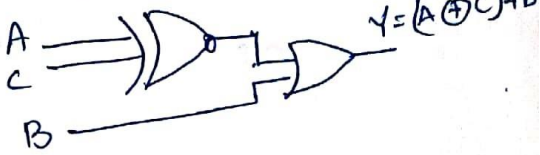
8. Draw the logic diagram to implement the following Boolean expressions

i) $Y = A+CD+ABC$
$= A(1+BC)+CD = A+CD$

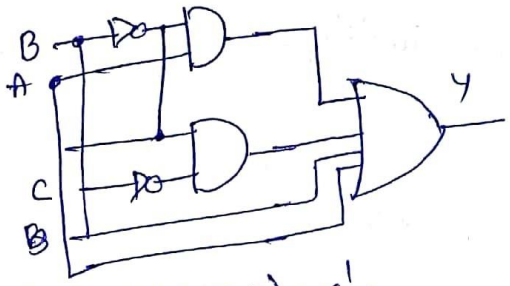




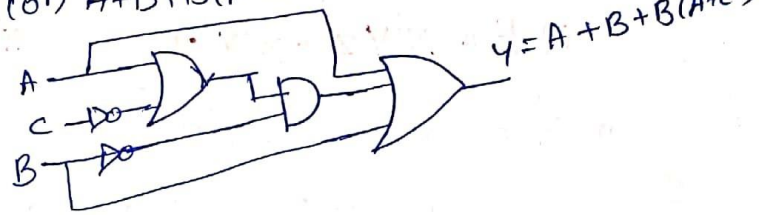
ii) $Y = (A \oplus C)' + B$



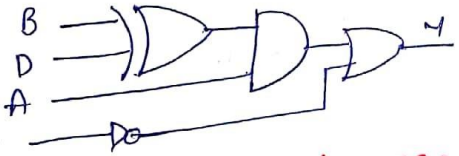
iii) $Y = A+B+B'(A+C')$.
$= A+B+B'A+B'C'$



(or) $A+B+B'(A+C')$



iv) $Y = A(B \oplus D)+C'$.



9. Find $(3250)_{10} - (72532)_{10}$ using 10's complement.

Sol:- given Subtraction of larger no. from smaller no. using 10's comp.

Step 1:- Find 10's complement of larger no.

9's complement $(q^n - 1) - N$.

$(10^5 - 1) - 72532$

$$\begin{array}{r} 99999 \\ -72532 \\ \hline 27467 \\ +\quad\ 1 \\ \hline 27468 \end{array}$$

10's comp.

Step 2:- Add 10's comp. to smaller no.

$$\begin{array}{r} 27468 \\ 3250 \\ \hline (30718)_{10} \end{array}$$

Step 3:- Ans. is in 2's complement form. To get the answer in the true form take the 1@'s comp. and assign -ve sign.

ANS :- 30718

9's comp $(10^5-1)-N$ = 99999 − 30718 = 69281

10's comp + 1 = 69282

Assign -ve sign — 69282

verify.
-72532
3250
-69282.

w. Find the complement of the following expressions

(i) $F_1 = x'yz' + x'y'z$ ii) $F_2 = x(y'z' + yz)$

i) $F_1' = (x'yz' + x'y'z)'$

$= (x'yz')' \cdot (x'y'z)'$ [∵ from duality].

$= (x + y' + z)(x + y + z')$.

ii) $F_2' = [x(y'z' + yz)]'$ (or) $[(xy'z') + (xyz)]'$

$= (x)' + (y'z')' \cdot (yz)'$ $= (\bar{x} + y + z)(x' + y' + z')$.

$= x' + [(y+z)(y'+z')] = (\bar{x} + y + z)(x' + y' + z')$.

a+(bc)
(a+b)
(a+c)

ii) $F_3 = (x + \bar{y} + z)(\bar{x} + \bar{z})(x + y)$.

$F_3' = [(x + \bar{y} + z)(\bar{x} + \bar{z})(x + y)]'$

$= (x + \bar{y} + z)' + (\bar{x} + \bar{z})' + (x + y)'$

$= (\bar{x} \cdot y \cdot \bar{z}) + (xz) + (\bar{x}\bar{y})$.

$= \bar{x}y\bar{z} + xz + \bar{x}\bar{y}$.

iv) $F_4 = (AB' + C)D' + E$

$(F_4)' = [(AB' + C)D' + E]'$

$= [(AB' + C)D']' \cdot E'$.

$= [(AB' + C)' + D] \cdot E'$

$= [[(AB')' \cdot C'] + D] E'$

$= [(A' + B) \cdot C' + D] E'$

$= [(\bar{A} + B)\bar{C} + D] E'$.

11. Convert gray code 101011 into its binary equivalent.

→Gray Code to Binary:- Take the MSB bit as it is and apply addition operation diagonally.

```
1 0 1 0 1 1
↓↗↓↗↓↗↓↗↓↗
1 1 0 0 1 0
```

ANS:- 110010.

12. Find $(1010100)_2 - (1000011)_2$ using 2's complement.

Sol:- step 1:- Identify smaller no. and larger no.

64 32 16 8 4 2 1
1 0 1 0 1 0 0 = 64+16+4 = $(84)_{10}$

1 0 0 0 0 1 1 = 64+2+1 = $(67)_{10}$.
64 32 16 8 4 2 1

Therefore, the given question is in the form of subtraction of smaller no. ~~and~~ from larger no.

step 2:- Find 2's complement of smaller no.

```
1 0 0 0 0 1 1
↓ ↓ ↓ ↓ ↓ ↓ ↓
0 1 1 1 1 0 0
          +1
-----------
0 1 1 1 1 0 1
```

2's comp.

step 3:- Add 2's complement of smaller no. to larger no.

```
  1 0 1 0 1 0 0
  0 1 1 1 1 0 1
① ↓ ↓ ↓ ↓ ↓ ↓
  0 0 1 0 0 0 1
```

step 4:- Neglect carry:-

step 5:- ANS:- 0 0 1 0 0 0 1.

verify

```
 84
-67
----
 17
```

0 0 1 0 0 0 1
64 32 16 8 4 2 1
16+1 = 17.

13. Convert $(10111011)_2$ into its equivalent gray code

Binary to Gray code:- Take the MSB bit as it is ~~called~~ add with adjacent digits and neglect carry.

```
1 0 1 1 1 0 1 1
↓ ↓ ↓ ↓ ↓ ↓ ↓ ↓
1 1 1 0 0 1 1 0
```

ANS:- 11100110

14. Convert $(4021.5)_5$ to its equivalent decimal.

$4\times5^3+0\times5^2+2\times5^1+1\times5^0\cdot5\times5^{-1}$

$= 125\times4+10+1\cdot5\times\frac{1}{5}$

$=500+10+1 \quad \therefore = 511.$

$=(511)_{10}$

15. Convert decimal number 22.64 to hexadecimal number.

$(22.64)_{10} \Rightarrow (?)_{16}$

16|22
1–6
$(16)_{16}$

$0.64\times16 = 10.24 = A$
$0.24\times16 = 3.84 = 3$
$0.84\times16 = 13.44 = D$
$0.44\times16 = 7.04 = 7$
$0.04\times16 = 10.24 = A$
$0.24\times16 =$

$(22.64)_{10} \rightarrow (16.A3D7A)_{16}$.

16. Find 2's complement of $(1010011)_2$

0 1 0 1 1 0 0
+ 1
0 1 0 1 1 0 1

ANS :- 0101101.

17. Encode the decimal number 365 in.

i) Binary ii) BCD iii) ASCI iv) Excess-3.

(i) $(365)_{10} = (\quad)_2$.

2|365
2|182-1
2|91-0
2|45-1
2|22-1
2|11-0
2|5-1
2|2-1
1-0

$\therefore (365)_{10} = (101101101)_2$

(ii) $(365)_{10} = (\quad)_{BCD}$.

3 6 5
$(0011\ 0110\ 0101)_{BCD}$.

$\therefore (365)_{10} = (0011\ 0110\ 0101)_{BCD}$.

iii) ASCII ⇒ (365) = 33 A36H 35H

(0110011 0110110 0110101)ASCII

iv) Excess-3

$(365)_{10}$ = 3 6 5

+3 +3 +3

6 9 8

↓ ↓ ↓

0110 1001 1000

18) a) Convert the following to decimal & then to octal.

i) 4234_{16} ii) 10010011

i) → Hexadecimal to decimal :-

$(4234)_{16} = 4\times16^3+2\times16^2+3\times16^1+4\times16^0$

$= 16384+512+48+4 = (16948)_{10}$

$\therefore \boxed{(4234)_{16} = (16948)_{10}}$

→ Hexadecimal to octal :-

$(4234)_{16}$ = 0100 0010 0011 0100

0 4 1 0 6 4

$\therefore \boxed{(4234)_{16} = (041064)_8}$

ii) → Binary to decimal :-

$(10010011)_2 = 1\times2^7+0\times2^6+0\times2^5+1\times2^4+0\times2^3+0\times2^2+1\times2^1+1\times2^0$

$= 128+16+2+1 = (147)_{10}$.

$\therefore \boxed{(10010011)_2 = (147)_{10}}$

→ Binary to octal

$(10010011)_2$ = 10 010 011

= 2 2 3

$\therefore \boxed{(10010011)_2 = (223)_8}$

(b) Obtain the truth table for the function $F = xy + xy' + y'z$

x	y	z	xy'	xy	xy'	$y'z$	F
0	0	0	1	0	0	0	0
0	0	1	1	0	0	1	1
0	1	0	0	0	0	0	0
0	1	1	0	0	0	0	0
1	0	0	1	0	1	0	1
1	0	1	1	0	0	1	1
1	1	0	0	1	0	0	1
1	1	1	0	1	0	0	1

19.a) Convert the fig to decimal and then to hexadecimal.

(i) $(1234)_8$ ii) $(11001111)_2$

(i) $(1234)_8 \Rightarrow (?)_{10}$

$= 1\times8^3 + 2\times8^2 + 3\times8^1 + 4\times8^0$

$= 512 + 128 + 24 + 4 = (668)_{10}$

512
128
28
+4
668

$\therefore \boxed{(1234)_8 = (668)_{10}}$

→ decimal to hexadecimal

$(668)_{10} = (?)_{16}$: 16 | 668 ; 16 | 41 - 12 (C) ; 2 - 9

$(668)_{10} = (29C)_{16}$

ii) $(11001111)_2$ to $(?)_{10}$: (128 64 32 16 8 4 2 1)

$= 1\times2^7 + 1\times2^6 + 0\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0$

$= 128 + 64 + 8 + 4 + 2 + 1 = (207)_{10}$

1
128
64
15
207

$\therefore \boxed{(11001111)_2 = (207)_{10}}$

$(207)_{10} = (?)_{16} \Rightarrow$ 16 | 207 ; 12 - F ; C - F

$\therefore \boxed{(207)_{10} = (CF)_{16}}$

b) Find the complement of the flg boolean fun. and reduce into minimum number of literals $Y = (BC' + A'D)(DB' + CD')$.

$$Y = (BC' + A'D)(DB' + CD')$$
$$= BC' \cdot DB' + BC'CD' + A'B'D \cdot D + A'CDD'$$
$$= 0 + 0 + A'B'D + D.$$
$$= A'B'D$$
$$Y' = (A'B'D)'$$
$$= (A')' + (B')' + D'.$$
$$= A + B + D'.$$

∴ The complement of the given boolean function is $A+B+D'$.

20.a) Show that dual of the exclusive-OR is equal to its complem

Sol:- Exclusive-OR function $Y = A'B + AB'$.

dual of Ex-OR is $Y = (A+\bar{B})(\bar{A}+B)$.

complement Ex-OR is $Y = (A'B + AB')'$

$$= (\bar{A}B)' \cdot (AB')'$$
$$= (A+\bar{B}) \cdot (\bar{A}+B).$$

∴ Dual of Ex-OR = complement of XOR.

(b) Convert the decimal number 1973 to base 3, base 5 & base 7

i) $(1973)_{10} = (?)_3$

3 | 1973	
3 | 657	-2
3 | 219	-0
3 | 73	-0
3 | 24	-1
3 | 8	-0
	2 -2

∴ $(1973) = (2201002)_3$

ii) $(1973)_{10} = (?)_5$

5 | 1973	
5 | 394	-3
5 | 78	-4
5 | 15	-3
	3 -0

∴ $(1973)_{10} = (30343)_5$

iii) $(1973) = (?)_7$

7 | 1973	
7 | 281	-6
7 | 40	-1
	5 -5

∴ $(1973)_{10} = (5516)_7$

Q1. Perform the following operations using 2's complement method: i) 48-23 ii) 23-48.

i) 48-23.

$(48)_{10} = (110000)_2$

$(23) = (010111)_2$.

2 | 48
2 | 24 - 0
2 | 12 - 0
2 | 6 - 0
2 | 3 - 0
1 - 1

2 | 23
2 | 11 - 1
2 | 5 - 1
2 | 2 - 1
1 - 0

step1:- Find 2's complement of smaller no.

$(23)_{10} \Rightarrow$ 1's comp + 1 = 101000 + 1 = $(101001)_2$

step2:- Add 2's complement of smaller no. to the larger no.

```
  110000
① 101001
  011001
```

step3:- Neglect carry. 011001 is the ans. i.e., $(25)_{10}$.

ii) (23-48)

step 1:- Find 2's complement to the larger number.

$(48)_{10} = 110000 \Rightarrow$ 2's comp. $\Rightarrow$ 1's comp + 1 = 001111 + 1 = 010000

= 010000

step 2:- Add 2's complement to the smaller number

```
  010111
  010000
+ ------
  100111
```

step 3:- The ans is in 2's complement form. To get the ans. take 2's comp. & assign negative sign.

$100111 \rightarrow 011000 + 1 = 011001 = (-25)_{10}$.

(32 16 8 4 2 1)

(7-1)

22. Perform the following operations using 2's complement method.

i) $(+55)-(+15) = 55-15$.

$55 = (110111)_2$

$15 = (1111)_2$

2|55
2|27-1
2|13-1
2|6-1
2|3-0
1-1

Step 1:- Find 2's complement of smaller number.

$(15)_{10} \Rightarrow (001111)_{10}$

2|15
2|7-1
2|3-1
1-1

2's comp = 1's + 1 = 110000 + 1 = 110001

55
-15
40

Step 2:- Add 2's comp. of smaller to larger.

```
  110111
  110001
① -------
  101000
```

Step 3:- neglect carry and ans is $101000 = (40)_{10}$.

ii) $(-55)-(-15) = -55+15 = 15-55$.

Step 1:- Find 2's complement of larger no.

$(55)_{10} = (110111)_2$

2's comp = 1's comp + 1 = 001000 + 1 = 001001

Step 2:- Add 2's complement of larger no. to smaller no.

```
  001111
  001001
  ------
  011000
```

Step 3:- The ans. is in 2's comp. form. To get the ans. take 2's comp. of ans. and assign -ve sign.

$011000 \rightarrow 100111$

```
  100111
  000001
  ------
  101000
```

$\rightarrow (-40)_{10}$

23. Is it possible to construct a 5411 weighted code and also 6321 weighted code? justify your answer.

Consider 5411 as a weighted code.

decimal no.	5411	6321
0	0000	0000
1	0001	0001
2	0011	0010
3	x	0100
4	0100	0101
5	0101	0110
6	1001	1000
7	1011	1001
8	x	1010
9	1100	1100

∴ By using 5411 we can't get a weight for 3 and 8 numbers. So, it is not a weighted code.

24. Find the complement of the following expressions.

i) $F_1 = x'yz' + x'y'z$

$(F_1)' = (x'yz' + x'y'z)'$

$= (x'yz')' \cdot (x'y'z)'$

$= (x + y' + z)(x + y + z')$.

$F_2 = x(y'z' + yz)$

$F_2' = [x(y'z' + yz)]'$

$= x' + (y'z')' \cdot (yz)'$

$= x' + (y + z) \cdot (\bar{y} + \bar{z})$.

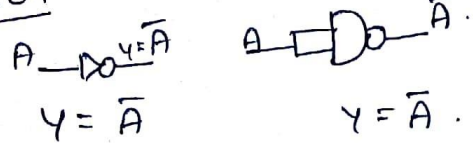
iii) ~~$F_3 = (AB' + C)D' + E$~~

25) What are Universal Gates? Realize AND, OR, NOT, XOR gates using Universal Gates?

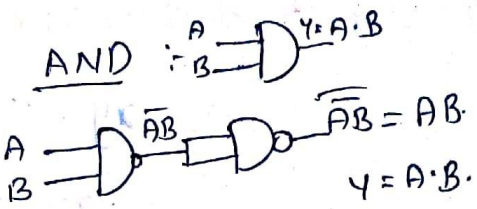
Ans: A universal gate is a gate which can implement any boolean function (or) logic gate without need of an other logic gate. ex: NAND & NOR gates.

Using NAND Gate:-

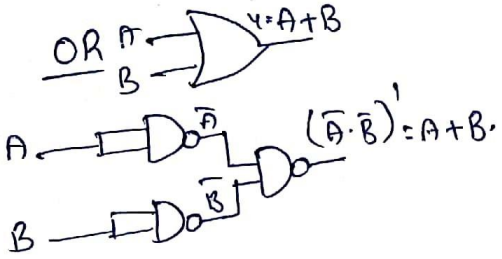
NOT



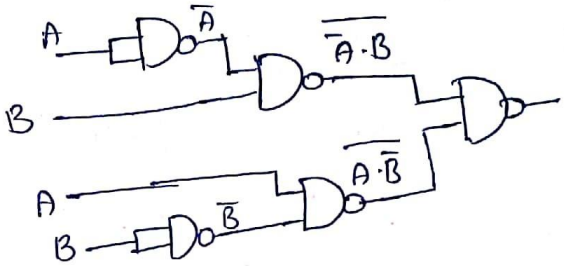
AND :-



OR

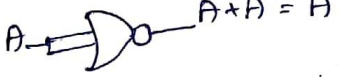


XOR Gate:-

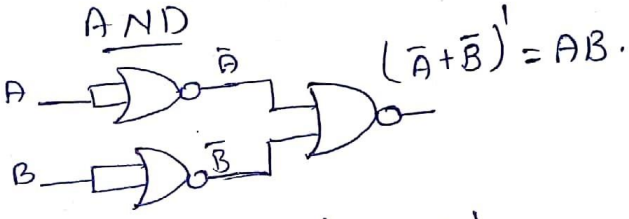


Using NOR Gate:-

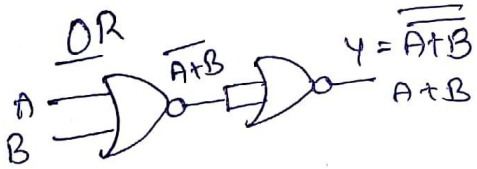
NOT



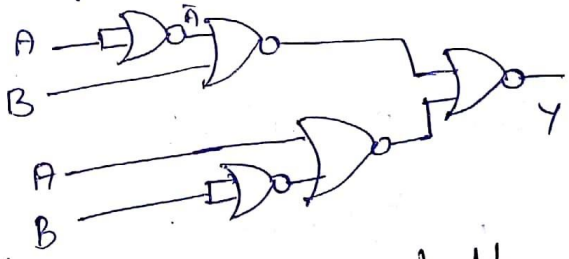
AND



OR



XOR $Y = A'B + AB'$



26) Reduce the following boolean expressions into the indicated number of literals.

i) $A'c' + ABc + Ac'$ to 3 literals.

$F = A'c' + ABc + Ac'$

$= c'(A+A') + ABc$

$= c' + ABc$

$= AB \cdot c + c'$

$= ABc' + c \cdot c'$ (∵ using distributive law).

$= ABc'$.

ii) $(x'.y'+z)'+z+xy+wz$ to 3 literals.

$(\bar{x}.\bar{y}+z)'+z+xy+wz.$

$[(\bar{x}\bar{y})'.z']+z+xy+wz.$

$[(x+y).z']+z+xy+wz.$

$xz'+yz'+z+xy+wz.$

$xz'+yz'+z(1+w)+xy.$

$xz'+yz'+z+xy.$

$xz'+(y+z)(z+z')+xy.$

$xz'+(y+z)+xy. = xz'+y+z+xy.$

~~$(xz'+xy)(y+z).$~~ $= xz'+y(1+x)+z.$

$= xz'+y+z.$

$= (x+z)(z+z')+y.$

$= (x+z)(1)+y.$

$= x+y+z.$

AB+C
(A+C)(A+B.

iii) $\bar{A}B(\bar{D}+\bar{C}D)+B(A+\bar{A}CD)$ to 1 literal.

$= \bar{A}B\bar{D}+\bar{A}B\bar{C}D+AB+\bar{A}BCD$

$= \bar{A}B\bar{D}+\bar{A}BD(C+\bar{C})+AB.$

$= \bar{A}B\bar{D}+\bar{A}BD+AB.$

$= \bar{A}B(D+\bar{D})+AB.$

$= \bar{A}B+AB.$

$= B(A+\bar{A}) = B.$

iv) $(\bar{A}+C)(\bar{A}+\bar{C})(A+B+C'D)$ to 4 literals.

$\Rightarrow (\bar{A}\bar{A}+\bar{A}\bar{C}+C\bar{A}+C.\bar{C})(A+B+\bar{C}D)$

$\Rightarrow (0+\bar{A}\bar{C}+\bar{A}C+0)(A+B+\bar{C}D).$

$\Rightarrow (\bar{A}\bar{C}+\bar{A}C)(A+B+\bar{C}D).$

$\Rightarrow A\bar{A}\bar{C}+B\bar{A}\bar{C}+\bar{C}D\bar{A}\bar{C}+\bar{A}CA+\bar{A}C\bar{C}B+\bar{A}CD\bar{C}$

$\Rightarrow 0+B\bar{A}\bar{C}+\bar{A}\bar{C}D+\bar{A}BC+0$

~~$+B$~~

$\Rightarrow \bar{A}BC+\bar{A}\bar{C}B+\bar{A}\bar{C}D.$

$\Rightarrow \bar{A}B(C+\bar{C})+\bar{A}\bar{C}D = \bar{A}B+\bar{A}\bar{C}D$

$= \bar{A}[B+\bar{C}D]$

UNIT - 2

1) State the distributive property of Boolean algebra.

The distributive property states that AND ing several variables and OR ing the result With a single variable is equivalent to OR ing the single variable with each of the the several Variables and then AND ing the sums. The distributive property is: A+BC= (A+B) (A+C)

2) State De Morgan's theorem.

De Morgan suggested two theorems that form important part of Boolean algebra. They are,

1) The complement of a product is equal to the sum of the complements. (AB)' = A' + B'

2) The complement of a sum term is equal to the product of the complements. (A + B)' = A'B'

3) Simplify the following expression Y = (A + B) (A + C') (B' + C')

Y = (A + B) (A + C') (B' + C')

= (AA' + AC +A'B +BC) (B' + C') [A.A' = 0]

= (AC + A'B + BC) (B' + C')

= AB'C + ACC' + A'BB' + A'BC' + BB'C + BCC'

= AB'C + A'BC'

4) Show that (X + Y' + XY) (X + Y') (X'Y) = 0

(X + Y' + XY)(X + Y')(X'Y) = (X + Y' + X) (X + Y') (X' + Y) [A + A'B = A + B]

= (X + Y') (X + Y') (X'Y) [A + A = 1]

= (X + Y') (X'Y) [A.A = 1]

= X.X' + Y'.X'.Y

= 0 [A.A' = 0]

5) Prove that ABC + ABC' + AB'C + A'BC = AB + AC + BC

ABC + ABC' + AB'C + A'BC=AB(C + C') + AB'C + A'BC

=AB + AB'C + A'BC

=A(B + B'C) + A'BC

=A(B + C) + A'BC

=AB + AC + A'BC

=B(A + C) + AC

=AB + BC + AC

=AB + AC +BC ...Proved

6) Convert the given expression in canonical SOP form Y = AC + AB + BC

Y = AC + AB + BC

=AC (B + B') + AB (C + C') + (A + A') BC

=ABC + ABC' + AB'C + AB'C' + ABC + ABC' + ABC

=ABC + ABC' +AB'C + AB'C' [A + A =1]

7) Define duality property.

Duality property states that every algebraic expression deducible from the postulates Of Boolean algebra remains valid if the operators and identity elements are interchanged. If the dual of an algebraic expression is desired, we simply interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

8) Find the complement of the functions F1 = x'yz' + x'y'z and F2 = x (y'z' + yz). By applying De-Morgan's theorem.

F1' = (x'yz' + x'y'z)' = (x'yz')'(x'y'z)' = (x + y' + z)(x + y +z') F2' = [x (y'z' + yz)]' = x' + (y'z' + yz)'

= x' + (y'z')'(yz)'

= x' + (y + z) (y' + z')

9) Simplify the following expression Y = (A + B) (A = C) (B + C)

= (A A + A C + A B + B C) (B + C)

= (A C + A B + B C) (B + C)

= A B C + A C C + A B B + A B C + B B C + B C C = A B C

10) What are the methods adopted to reduce Boolean function?

i) Karnaug map ii) Tabular method or Quine Mc-Cluskey method

iii) Variable entered map technique.

11) State the limitations of karnaugh map.

ii) Generally it is limited to six variable map (i.e) more then six variable involving expression are not reduced.

iii)The map method is restricted in its capability since they are useful for simplifying only Boolean expression represented in standard form.

12) What is a karnaugh map?

A karnaugh map or k map is a pictorial form of truth table, in which the map diagram is made up of squares, with each squares representing one minterm of the function.44) Find the minterms of the logical expression

Y = A'B'C' + A'B'C + A'BC + ABC' Y = A'B'C' + A'B'C + A'BC + ABC'

=m0 + m1 +m3 +m6

=_m (0, 1, 3, 6)

13) Write the maxterms corresponding to the logical expression Y = (A + B + C') (A + B' + C') (A' + B' + C)

= (A + B + C') (A + B' + C') (A' + B' + C)

=M1.M3.M6

= M (1, 3, 6)

14) Define prime implicant in k map

A prime implicant in k map is a product term obtained by obtaining the maximum possible number of adjacent squares in the map.

15) Define essential prime implicant in k map

If a minterm in a square is covered by only one prime implicant that prime implicant is called essential prime implicant

16) Define non- essential prime implicant in k map

If a minterm in a square is covered by more than only one prime implicant then that prime implicant is called non-essential prime implicant.

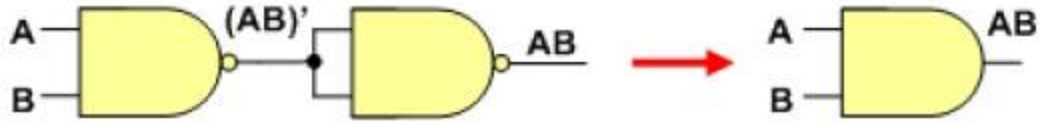
17) Draw two graphic symbols of NAND and name them.

NAND **INPUT BUBBLED OR GATE**

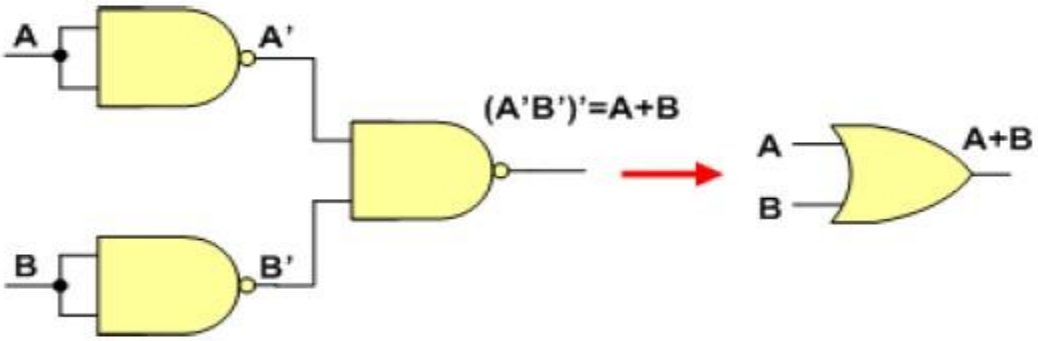
18) Draw two graphic symbols of NOR and name them.

NOR GATE **INPUT BUBBLED NAND GATE**

19) Implementing AND Using only NAND Gates



20) Implementing OR Using only NAND Gates



21) Prove that the logical sum of all minterms of a Boolean function of 2-ariable is 1

Consider two variables as A and B. For two variables A and B minterms are: A′B′,A′B,AB′,AB.
The logical sum of these minterms are given by
F= A′B′+A′B+AB′+AB
= A′(B′+B)+A(B′+B) (B′+B=1)
= A′(1)+A(1) (A′+A=1)
F=1
Hence it is to be proved

UNIT - 3

1) Define combinational logic.

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

2) Write the design procedure for combinational circuits.

- The problem definition
- Determine the number of available input variables & required O/P variables.
- Assigning letter symbols to I/O variables
- Obtain simplified Boolean expression for each O/P.
- Obtain the logic diagram.

3) Define half adder and full adder.

The logic circuit that performs the addition of two bits is a half adder. The circuit that performs the addition of three bits is a full adder.

4) Define Decoder.

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

5) What is binary decoder?

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2n out puts lines.

6) Define Encoder.

An encoder has 2n input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

7) What is priority Encoder?

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

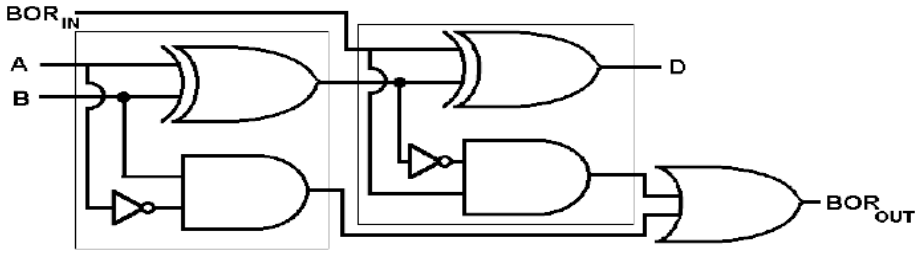
8) Define multiplexer.

Multiplexer is a digital switch. If allows digital information from several sources to be routed onto a single output line.

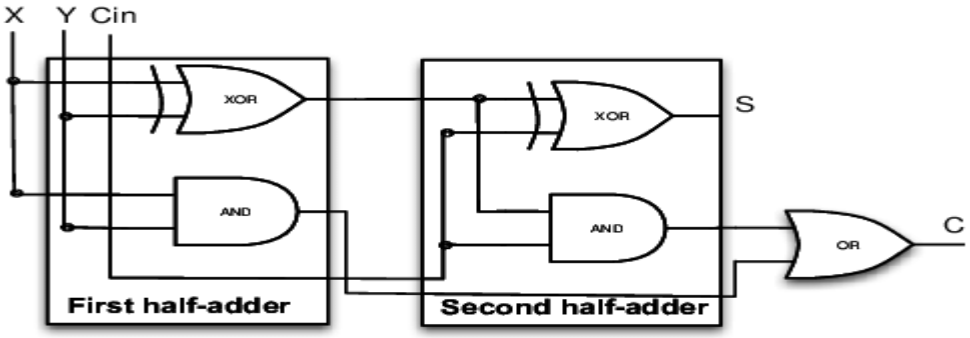
9) What do you mean by comparator?

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers

10) Design a full subtractor by using 2-half subtractor



11) Design a full adder by using 2-half adder



12) What are Application of Decoder

- The **Decoders** were used in analog to digital conversion in analog **decoders**.
- Used in electronic circuits to convert instructions into CPU control signals.
- They mainly used in logical circuits, data transfer.

13) What is the use of Enable in decoder?

A **Decoder** with **Enable** input can function as a demultiplexer. A demultiplexer is a circuit that receives information from a single line and directs it to one of possible output lines.

14) WHY AND gate is used in decoder?

It is convenient to **use** an AND **gate** as the basic **decoding** element for the output because it produces a "HIGH" or logic "1" output only when all of its inputs are logic "1". As a NAND **gate** produces the AND operation with an inverted output, the NAND **decoder** looks like this with its inverted truth table.

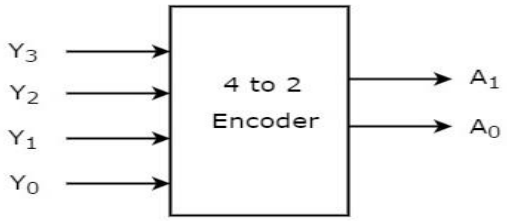
15) What is difference between decoder and multiplexer?

- **Multiplexer** is a device which consists of multiple input channels thru single line while **decoders** consist of multiple inputs passing thru multiple outputs.
- **Multiplexer** converts inputs from unary codes (initial) to binary codes while **decoder** converts binary codes to inputs.

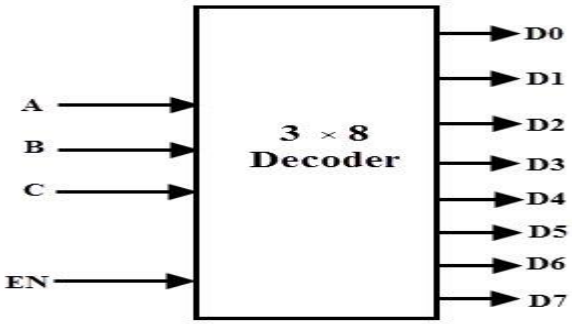
16) What are the applications of encoder and decoder?

In digital electronic projects, the **encoder and decoder** play an important role. It is used to convert the data from one form to another form. Generally, these are frequently used in the communication systems like telecommunication, networking, and transfer the data from one end to the other end

17) Draw the block diagram 4*2 encoder



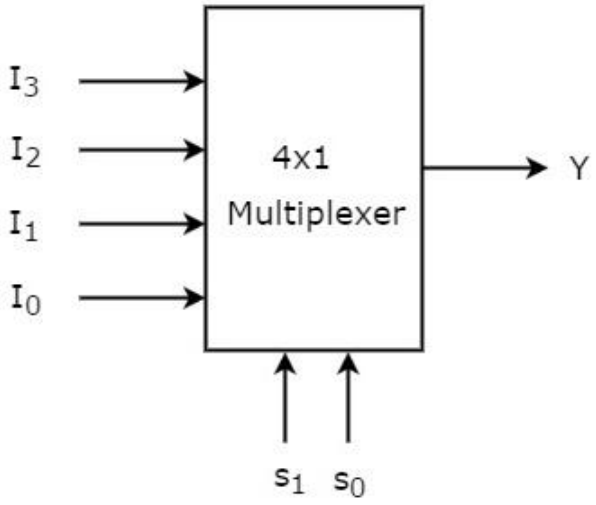
18) Draw the block diagram 3*8decoder



19) What is difference between multiplexer and demultiplexer?

A **multiplexer** is a combinational circuit that provides single output but accepts multiple data inputs. A **demultiplexer** is a combinational circuit that takes single input but that input can be directed through multiple outputs. ... It is 1 to N device and thus behaves as data distributor.

20) Draw the block diagram 4*1multiplexer.



UNIT – 4

1. What are the classifications of sequential circuits?
The sequential circuits are classified on the basis of timing of their signals into two types. They are,
1) Synchronous sequential circuit. 2) Asynchronous sequential circuit.

2. Define Flip flop.
The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

3. What are the different types of flip-flop?
There are various types of flip flops. Some of them are mentioned below they are,
(1) RS flip-flop (2) SR flip-flop (3) D flip-flop
(4) JK flip-flop (5) T flip-flop

4. What is the operation of RS flip-flop?
- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change
- When both the inputs R and S are high the output is unpredictable.

5. What is the operation of SR flip-flop?
- When R input is low and S input is high the Q output of flip-flop is set.
- When R input is high and S input is low the Q output of flip-flop is reset.
- When both the inputs R and S are low the output does not change.
- When both the inputs R and S are high the output is unpredictable.

6. What is the operation of D flip-flop?
In D flip-flop during the occurrence of clock pulse if D=1, the output Q is set and if D=0, the output is reset.

7. What is the operation of JK flip-flop?
- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the Flip-flop (ie) the output toggle on the next positive clock edge.

8. What is the operation of T flip-flop?
T flip-flop is also known as Toggle flip-flop.
- When T=0 there is no change in the output.
- When T=1 the output switch to the complement state (ie) the output toggles.

9. Define race around condition.

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called race around condition'.

10. What is edge-triggered flip-flop?

The problem of race around condition can solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

11. What is a master-slave flip-flop?

A master-slave flip-flop consists of two flip-flops where one circuit serves as a master and the other as a slave.

12. Explain the flip-flop excitation tables for RS FF.

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

- _ 0_0 transition: This can happen either when R=S=0 or when R=1 and S=0.
- _ 0_1 transition: This can happen only when S=1 and R=0.
- _ 1_0 transition: This can happen only when S=0 and R=1.
- _ 1_1 transition: This can happen either when S=1 and R=0 or S=0 and R=0.

13. Explain the flip-flop excitation tables for JK flip-flop

In JK flip-flop also there are four possible transitions from present state to next state.They are,

- _ 0_0 transition: This can happen when J=0 and K=1 or K=0.
- _ 0_1 transition: This can happen either when J=1 and K=0 or when J=K=1.
- _ 1_0 transition: This can happen either when J=0 and K=1 or when J=K=1.
- _ 1_1 transition: This can happen when K=0 and J=0 or J=1.

14. Explain the flip-flop excitation tables for D flip-flop

In D flip-flop the next state is always equal to the D input and it is independent of the present state. Therefore D must be 0 if Qn+1 has to 0, and if Qn+1 has to be 1 regardless the value of Qn.

15. Explain the flip-flop excitation tables for T flip-flop

When input T=1 the state of the flip-flop is complemented; when T=0, the state of the Flip-flop remains unchanged. Therefore, for 0_0 and 1_1 transitions T must be 0 and for 0_1 and 1_0 transitions must be 1.

16. Define sequential circuit.

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

17. Give the comparison between combinational circuits and sequential circuits.
Combinational circuits Sequential circuits Memory unit is not required Memory unity is Required Parallel adder is a combinational circuit Serial adder is a sequential circuit.

18. What do you mean by present state?
The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

19. What do you mean by next state?
The present state and the external inputs determine the outputs and the next state of the sequential circuit.

20. State the types of sequential circuits?
1. Synchronous sequential circuits 2. Asynchronous sequential circuits

21. Define synchronous sequential circuit
In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

22. Define Asynchronous sequential circuit?
In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

23. Give the comparison between synchronous & Asynchronous sequential circuits?
Synchronous sequential circuits Asynchronous sequential circuits. Memory elements are locked flip-flops Memory elements are either unlocked flip - flops or time delay elements.

24. What is race around condition?
In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

25. Give the comparison between synchronous & Asynchronous counters.
Asynchronous counters
- In this type of counter flip-flops are Connected in such a way that output of 1st Flip-flop drives the clock for the next Flip-flop
- All the flip-flops are not clocked simultaneously

Synchronous counters
- In this type there is no connection between output of first flip-flop and clock input of the next flip – flop
- All the flip-flops are clocked simultaneously

UNIT – 5

1. Explain ROM.

A read only memory (ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit Combination of the input variables is called an address. Each bit combination that comes out of the output lines
is called a word. The number of distinct addresses possible with n input variables is 2n.

2. What are the types of ROM?

1. Masked ROM.
2. PROM
3. EPROM
4. EEPROM
5. FLASH

3. Explain PROM.

PROM (Programmable Read Only Memory) it allows user to store data or program.
PROMs use the fuses with materiallike nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20μs.The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

4. Explain EPROM.

EPROM (Erasable Programmable Read Only Memory) EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

5. Explain EEPROM.

EEPROM (Electrically Erasable Programmable Read Only Memory). EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating
gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

6. Define address and word:

In a ROM, each bit combination of the input variable is called on address. Each bit combination that comes out of the output lines is called a word.

7. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generates all the min terms as in the ROM.

8. What is mask - programmable?
With a mask programmable PLA, the user must submit a PLA program table to the manufacturer.

9. What is field programmable logic array?
The second type of PLA is called a field programmable logic array. The user by means of certain recommended procedures can program the EPLA.

10. List the major differences between PLA and PAL
PLA: Both AND and OR arrays are programmable and Complex Costlier than PAL
PAL: AND arrays are programmable OR arrays are fixed Cheaper and Simpler

11. Define PLD.
Programmable Logic Devices consist of a large array of AND gates and OR gates that Can be programmed to achieve specific logic functions.

12. Give the classification of PLDs.
PLDs are classified as PROM (Programmable Read Only Memory), Programmable Logic Array (PLA), Programmable Array Logic (PAL), and Generic Array Logic (GAL)

13. Define PROM.
PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates Connected to a decoder and a programmable OR array.

14. Define PLA.
PLA is Programmable Logic Array (PLA). The PLA is a PLD that consists of a Programmable AND array and a programmable OR array.

15. Define PAL.
PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.

16. Why was PAL developed?
It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.

17. What is CPLD?
CPLDs are Complex Programmable Logic Devices. They are larger versions of PLDs with a centralized internal interconnect matrix used to connect the device macro cells together.

18. Define bit, byte and word.
The smallest unit of binary data is bit. Data are handled in a 8 bit unit called byte. A complete unit of information is called a word which consists of one or more bytes.

19. How many words can a 16x8 memory can store?
A 16x8 memory can store 16,384 words of eight bits each

20. Define address of a memory.
The location of a unit of data in a memory is called address.

21. What is Read and Write operation?
The Write operation stores data into a specified address into the memory and the Read operation takes data out of a specified address in the memory.

22. Why RAMs are called as Volatile?
RAMs are called as Volatile memories because RAMs lose stored data when the power is turned OFF.

23. Define ROM.
ROM is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation.

24. Define RAM.
RAM is Random Access Memory. It is a random access read/write memory. The data can be read or written into from any selected address in any sequence.

25. Define Static RAM and dynamic RAM.
Static RAM use flip flops as storage elements and therefore store data indefinitely as long as dc power is applied. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without capacitors being recharged by a process called refreshing.

26. List basic types of programmable logic devices.
1. Read only memory 2. Programmable logic Array 3. Programmable Array Logic