Code : A1402 R18

II B.Tech I Semester (R18) Regular Examinations November 2019

DIGITAL LOGIC DESIGN

Time : 3 hours Max. Marks: 70

PART- A

(Compulsory Question 10 X 2 = 20M)

1 a Convert decimal 27.315 to binary.

b Find the minimal SOP expression of F = A'C + A'B + AB'C + BC.

c Define Essential Prime Implicants. with an example.

d Simplify the Boolean function *F(A,B,C) = Σm (0, 2, 3, 4, 6, 7)* using K-Map.

e Distinguish between combinational logic and sequential logic.

f Realize a full adder using two half adders and an OR gate.

g Draw the SR flip flop diagram with characteristic table?

h What is Ring Counter?

i Define RAM and ROM?

j Realize the following Boolean functions using a PROM. $F_1(A,B,C) = \Sigma m\ (0, 4, 7)$, $F_2(A,B,C) = \Sigma m(1,3,6)$.

PART- B

(Answer all the questions, Each carry 10M)

2 a Subtract the following using 1's and 2's complement and verify the result with decimal values.
(i) 111001 – 001010 (ii) 101011 – 100110 (iii) 11010 – 1101 (iv) 0011011 - 1010101

b Simplify the following Boolean expressions to a minimum number of literals.
(i) $X[Y+Z(XY+XZ)^1]$ (ii) $A^1B\ (D^1+C^1D) +B\ (A+A^1CD)$ to one literal.

(OR)

3 a Express the Boolean function *F(A, B, C, D)* $= \bar{B}D + \bar{A}D + BD$ as a Canonical Sum-of-minterms and Product of maxterms.

b Express the following numbers in decimal:
(i) $(10110.0101)_2$ (ii) $(16.5)_{16}$ (iii) $(26.24)_8$ (iv) $(DADA)_{16}$

4 a Find all the prime implicants for the following Boolean functions, and determine which are essential:
(i) F (w, x, y, z) = *Σm* (0, 2, 4, 5, 6, 7, 8, 10, 13, 15).
(ii) F (A, B, C, D) = *Σm* (1, 3, 6, 7, 8, 9, 12, 13, 14, 15).

b Minimize the following Boolean function F(w, x, y, z) = *Σm* (0, 4, 8, 9, 10, 11, 12, 14) using the k map.

(OR)

5 Obtain minimal expression for the switching function f *(A,B,C,D) = Σ m(0, 5, 7, 8, 9, 10, 11, 14, 15)* using Tabulation method.

6 a Design a combinational circuit with three inputs, x , y , and z , and three outputs, A, B , and C . When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is two less than the input.

b Construct a 4-to-16-line decoder with two 3-to-8-line decoders with enable input.

(OR)

7 a Design a full adder using 3 to 8 decoder and OR gate.

b Design the two bit comparator?

8 A sequential circuit with two D flip-flops A and B, two inputs, x and y ; and one output z is specified by the following next-state and output equations . A(t + 1) = xy + xB, B(t + 1) = xA + xB, z = A

i. Draw the logic diagram of the circuit.

ii. List the state table for the sequential circuit.

iii. Draw the corresponding state diagram.

(OR)

9 a Design a BCD synchronous counter using JK flip-flop.

b Draw the logic diagram of Serial In, Serial Out shift register and explain its operation.

10 a Draw a PLA circuit to implement the functions F1 = (AB + AC + ABC), F2 = (AC + AB + BC).

b Compare the architectures of PLA, PAL & PROM.

(OR)

11 a Implement the following functions using PAL $F_1(A,B,C) = \Sigma\ m(3, 5, 6, 7)$,
$F_2\ (A,B,C) = \Sigma m\ (2, 3, 4, 5,7)$

b Implement 4 bit binary to gray code converter using PROM.

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PART- A

(Compulsory Question)

1	a	Represent $(246)_{10}$ in Binary and BCD.
	b	Find the 2's complement of 11000011.
	c	Simplify the Boolean expression x'yz + xy'z' + xy'z using K-map.
	d	Simplify the Boolean function *F (A,B,C)= ΠM (3, 4, 6, 7)* using K-Map
	e	What is a priority encoder?
	f	Why a multiplexer is called a data selector?
	g	What is meant by race around condition in flip-flops?
	h	What are the basic types of shift registers?
	i	Implement the following Boolean functions using PAL. $F_1(A,B,C) = \Sigma m (4, 5, 6, 7)$ $F_2(A,B,C) = \Sigma m(2, 3, 4, 5)$.
	j	What are the types of ROMs?

UNIT-1

2	a	Reduce the following Boolean expressions to the indicated number of literals: i. AC + ABC + AC to three literals ii. (xy + z) + z + xy + wz to three literals iii. AB(D + CD) + B(A + ACD) to one literal iv. (A + C) (A + C) (A + B + CD) to four literals
	b	Express the complement of the following functions in sum-of-minterms form: i. F(A,B ,C, D) = Σm (2, 4, 7, 10, 12, 14) ii. F (x, y, z) = Σm (3, 5, 7).

(OR)

3	a	Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign. i. 10011 - 10010 ii. 100010 - 100110 iii. 1001 – 110101 iv. 101000 - 10101
	b	Obtain the Demorgans law and Duality Principle of the following Boolean expressions. (i) $(A\overline{B} + A\overline{C})(BC + B\overline{C})(ABC)$ (ii) $A\overline{B}C + \overline{A}BC + ABC$ (iii) $(\overline{ABC})(\overline{A + B + C})$

UNIT-II

4	a	Implement Ex-NOR function using only: (i) NAND gates. (ii) NOR gates.
	b	Implement the following Boolean function with basic gates: F (w,x, y, z) = Σm (1, 2, 3, 4, 5, 7)+d(0,9,12,14).

(OR)

5	a	Simplify the following Boolean functions and Implement the result with universal Gates: (a) F(A, B, C, D) = Σm (1, 3, 5, 7, 13, 15) (b) F(A, B, C, D) = *ΠM* (0,2,4,7,9,11,13,15).
	b	Obtain minimal expression for *f*(A, B, C, D,E) *= Σ (0, 1, 2, 8, 9, 15, 17, 21, 24, 25, 27, 31)* using tabulation method.

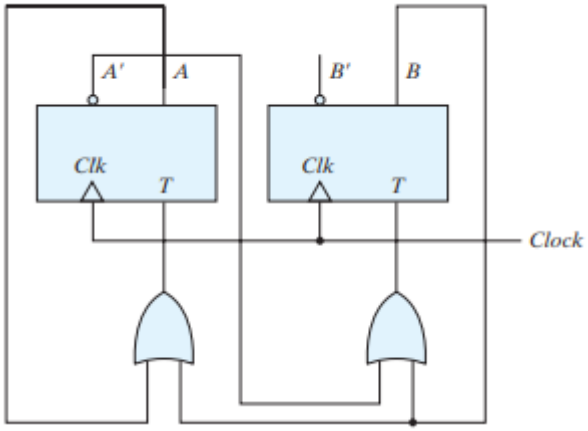
UNIT-III

6	a	Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable
	b	Design a Combinational circuit that accepts a three-bit binary number and generates an output binary number equal to the square of the input number.

(OR)

7	a	Implement the logic expression given below using F (A, B, C, D) = ∑m (0, 1, 3, 5, 8, 11, 12, 14, 15) (i) 16:1 MUX (ii) 8:1 MUX
	b	Illustrate the design procedure by taking BCD to excess-3 code converter as an example.

UNIT-IV

8		Derive the state table and the state diagram of the sequential circuit shown in below Figure. Explain the function that the circuit performs. 

(OR)

9	a	Convert the following Flip-Flop conversions. i. D flip-flop to T flip-flop. ii. SR flip-flop to JK flip-flop.
	b	Draw the logic diagram of a 4-bit bidirectional shift register and explain its operation.

UNIT-V

10	a	Design a combinational circuit using PLA, which accepts a 3-bit binary number as input and generates its equivalent Excess-3 code as output.
	b	Explain the architecture of FPGA.

(OR)

11	a	Tabulate the truth table for an 8X 4 ROM that implements the Boolean functions A(x, y, z) = (0, 3, 4, 6) ; B(x, y, z) = (0, 1, 4, 7); C(x, y, z) = (1, 5); D(x, y, z) = (0, 1, 3, 5, 7).
	b	Briefly discuss Flash memories.